HIGH EFFICIENCY SYNCHRONOUS DC-DC BUCK-BOOST CONVERTER WITH 4.3A SWITCHES

Description

The AP72200 is a high-current synchronous buck-boost converter providing high efficiency, excellent transient response, and high DC output accuracy. The targeted applications are smartphones, tablets, and other handheld devices. The AP72200 utilizes a four-switch H-bridge configuration to support buck and boost operation. The buck-boost provides at least 2A output current.

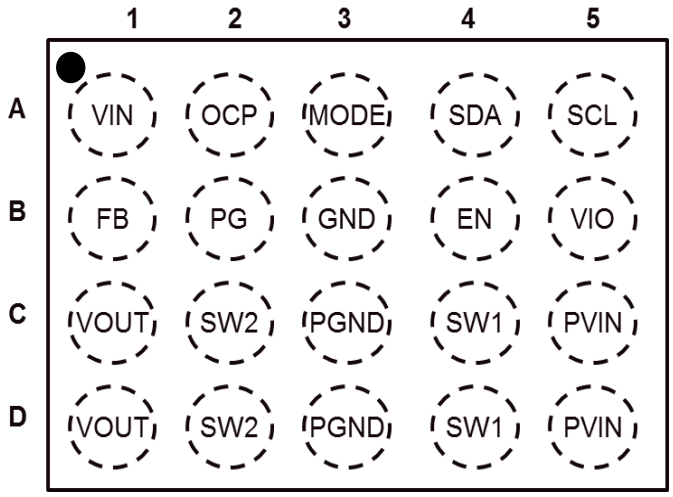
The current control scheme handles wide input/output voltage ratios and provides low external component count with outstanding performance in line/load transient response and seamless transition between buck and boost modes.

The AP72200 features I^2C compatible, two-wire serial interface consisting of a bidirectional serial-data line, SDA, and a serial-clock line, SCL. It supports SCL clock rates up to 3.4MHz.

The AP72200 also features UVLO, OTP, and OCP to protect the circuit.

This IC is available in a small 2.125mm × 1.750mm, 20 balls WLCSP package.

Pin Assignments



TOP VIEW
(BALLS SIDE DOWN)

Features

- V_{IN} 2.3V to 5.5V
- Output Voltage Range: 2.6V to 5.14V
- 2A Continuous Output Current for V_{OUT}=3.4V and V_{IN}>2.9V Efficiency Up to 97%
- 2.5MHz Switching Frequency
- I^2C Interface
- Selectable MODE PFM/PWM
- Ultrasonic Operation Programmable through I^2C
- Power Good Indicator with 5MΩ Internal Pull-Up
- Adjustable Overcurrent Limit
- Fully Protected for Overcurrent, Short Circuit, Reverse Current Protection, Overtemperature, and UVLO
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Applications

- Smartphones
- Tablets
- Portable Consumer Devices

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Typical Applications Circuit

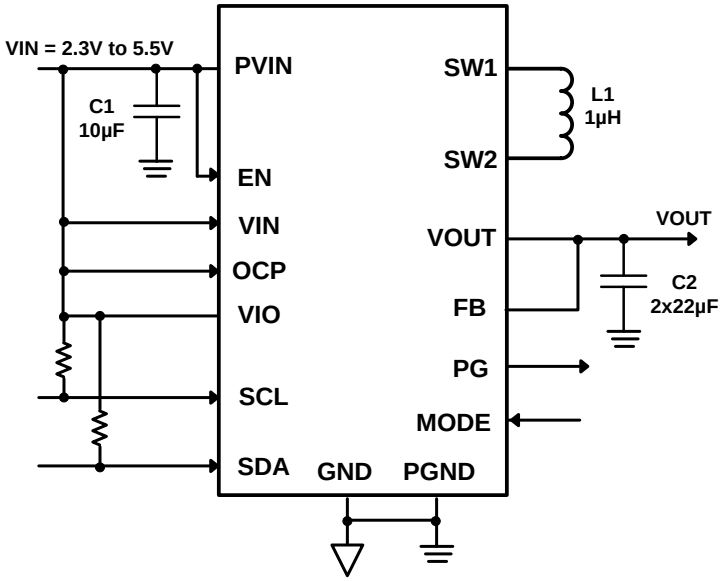
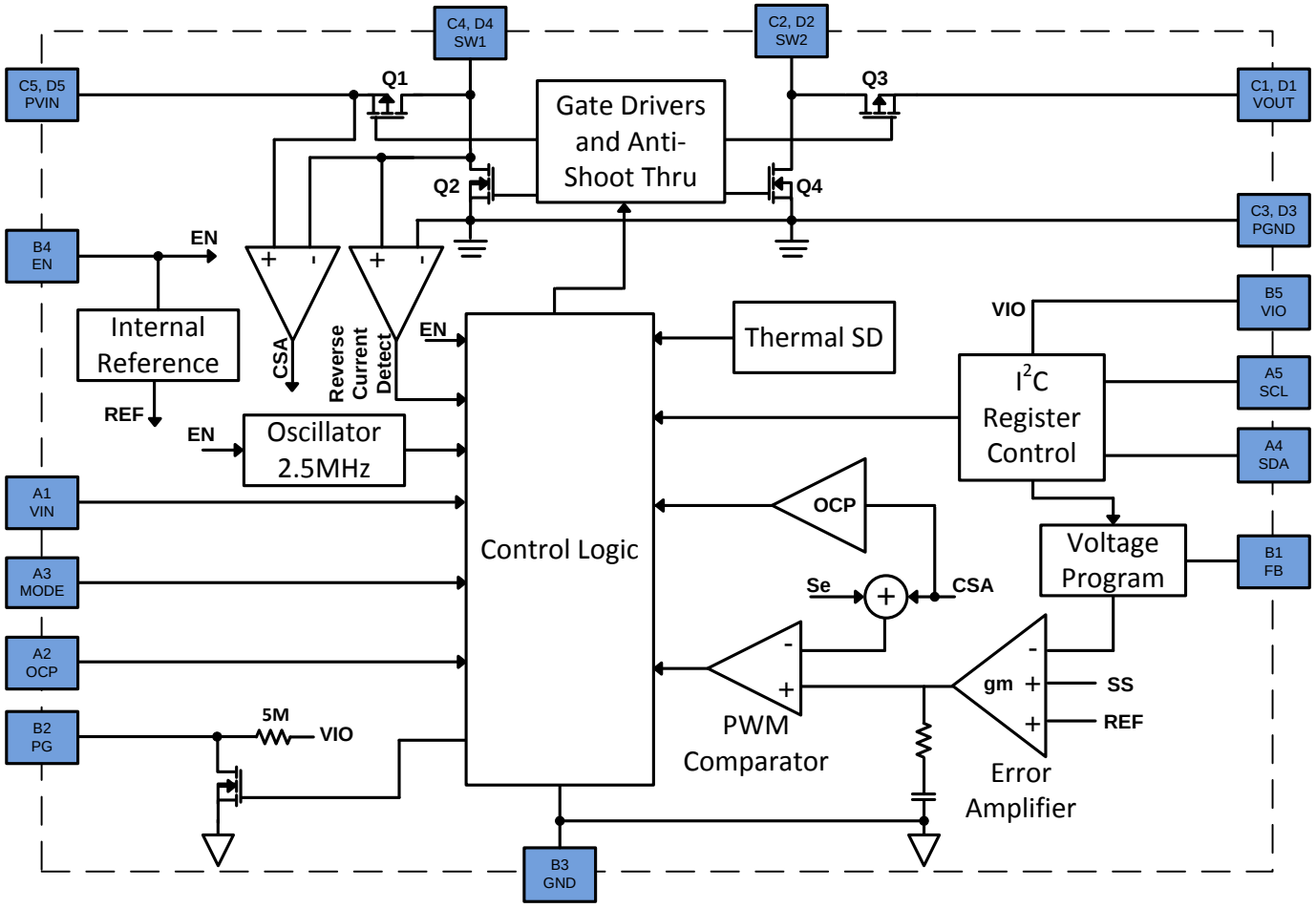


Figure 1 Typical Application Circuit

Pin Descriptions

Pin Name	Pin Number 20 BALLS	Function
VIN	A1	Input supply for the logic control circuitries.
OCP	A2	OCP program the current limit. LOW will set the OCP threshold to 2A. HIGH will set the OCP threshold to 4.3A. I^2C can override the MODE pin. See the register for more detail.
MODE	A3	MODE logic input. LOW for PFM operation. HIGH for forced PWM. There is an internal 5.5MΩ resistor from MODE and GND to set the IC in PFM if left floating. I^2C can override the MODE pin. See the register for more detail.
SDA	A4	I^2C Data I/O.
SCL	A5	I^2C Clock Input.
FB	B1	Feedback Input. FB senses the output voltage and regulates it. Connect FB to VOUT.
PG	B2	Open drain power-good output that is pulled to GND when the output voltage is out of its regulation limits or during soft-start interval. Active high by default. There is an internal 5MΩ pull-up resistor to VIO.
GND	B3	Analog ground that is used for control.
EN	B4	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator; low to turn it off.
VIO	B5	Input supply for the I^2C and PG internal pull-up resistor.
VOUT	C1, D1	Buck-Boost output.
SW2	C2, D2	Switch Node 2.
PGND	C3, D3	Power Ground.
SW1	C4, D4	Switch Node 1.
PVIN	C5, D5	Power Input. Bypass PVIN to GND with a 10µF capacitor to eliminate noise on the input to the IC. See Input Capacitor.

Functional Block Diagram



Absolute Maximum Ratings (Note 4) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Rating	Unit
V_{IN}, PV_{IN}	Supply Voltage	-0.3 to +7.0	V
V_{OUT}	Output Voltage	-0.3 to +6.0	V
V_{SW1},V_{SW2}	Switch Node Voltage	-1.0 to +7.0 (DC)	V
V_{SW1},V_{SW2}	Switch Node Voltage	-2.5 to +8.0 (20ns)	V
V_{IO}	I^2C Voltage	-1.0 to +7.0	V
All Other Pins	—	-0.3V to +7.0	V
T_J	Junction Temperature	+150	°C
T_L	Lead Temperature	+260	°C
ESD Susceptibility (Note 5)	—	—	—
HBM	Human Body Model	3000	V
CDM	Charged Device Model	1000	V

Notes: 4. Stresses greater than the 'Absolute Maximum Ratings' specified above may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions exceeding those indicated in this specification is not implied. Device reliability may be affected by exposure to absolute maximum rating conditions for extended periods of time.
5. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

Thermal Resistance (Note 6)

Symbol	Parameter	Rating		Unit
Θ_{JA}	Junction to Ambient	2.125mm × 1.750mm	50	°C/W
Θ_{JC}	Junction to Case	2.125mm × 1.750mm	2	°C/W

Note: 6. Test condition for WLSCSP: Device mounted on FR-4 substrate, four-layer PC board, 2oz copper, with minimum recommended pad layout

Recommended Operating Conditions (Note 7) (@T_A = +25°C, unless otherwise specified.)

Symbol	Parameter	Min	Max	Unit
PV_{IN}	Supply Voltage	2.3	5.5	V
T_A	Operating Ambient Temperature Range	-30	+85	°C

Note: 7. The device function is not guaranteed outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25°C, V_{IN} = PVIN = EN = 3.6V, unless otherwise specified.)

Min/Max limits apply across the recommended ambient temperature range, -30°C to +85°C and input voltage range 2.3V to 5.5V.

Buck-Boost Characteristics						
Symbol	**Parameter**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
I_{IN}	Shutdown Supply Current	V_{EN} = 0V	—	0.3	1	μA
I_{IN}	Supply Current (Quiescent)	V_{EN} = V_{IN}, Non-Switching, EN_PD BIT = 0	—	20	30	μA
		PFM, V_{EN} = V_{IN}, V_{IO}=0V, MODE=0	—	29	45	μA
		Ultrasonic Mode, V_{EN} = V_{IN}, V_{IO}=0V, MODE=0, BB_UMODE=1, BB_FPWM=0	—	180	250	μA
		PWM, V_{EN} = V_{IN}, V_{IO}=0V, MODE=1	—	9	15	mA
POR/UVLO	V_{IN} Power On Reset Voltage Threshold, Rising Edge	—	2.150	2.225	2.295	V
	Vin, Undervoltage Lock Out Threshold, Falling Edge	—	2.055	2.125	2.230	V
	Hysteresis	—	50	100	150	mV
$R_{DS(ON)1}$	High-Side Switch On-Resistance from PVIN to SW1	—	—	25	40	mΩ
$R_{DS(ON)2}$	Low-Side Switch On-Resistance from SW1 to PGND	—	—	25	40	mΩ
$R_{DS(ON)3}$	High-Side Switch On-Resistance from SW2 to VOUT	—	—	25	40	mΩ
$R_{DS(ON)4}$	Low-Side Switch On-Resistance from SW2 to PGND	—	—	25	40	mΩ
$R_{DISCHARGE}$	VOUT Soft Discharge On-Resistance	—	70	100	130	Ω
Leakage Current SW1/SW2	HS Q1 or HS Q3 Leakage Current	SW1 = 0V or SW2 = 0V. V_{IN}=5.5V, EN=0V	—	—	1	μA
I_{LIMIT}	Positive HS Current Limit, Q1	OCP=0V	1.7	2.0	2.3	A
		OCP=V_{IN}	3.9	4.3	4.7	A
I_{PFMPK}	PFM Peak Current Limit	—	0.85	1.00	1.15	A
I_{ZC}	Zero Cross Current Threshold	—	—	200	—	mA
I_{NLIMIT}	Negative LS Current Limit, Q2	—	1.4	2.0	2.6	A
F_{SW}	Oscillator Frequency	Continuous Switching Frequency at Both Buck and Boost Mode	2.1	2.5	2.9	MHz
		Ultrasonic Mode, BB_UMODE=1, BB_FPWM=0	20	27	—	KHz
V_{OUT}	Output Voltage Range	I^2C Programmable (20mV step)	2.60	—	5.14	V
	Default Output Voltage	I_{OUT}=0A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=1	3.366	3.400	3.434	V
	Output Accuracy	I_{OUT}=0A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=0	3.349	—	3.46	V
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	PFM, V_{IN}=2.3V-5.5V, I_{OUT}=0A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=0	—	1.3	—	mV/V
		Ultrasonic Mode, V_{IN}=2.3V-5.5V, I_{OUT}=0A, Address 0x04, V_{OUT} [6:0]=0x28, BB_UMODE=1, BB_FPWM=0	—	1.7	—	mV/V
		PWM, V_{IN}=2.3V-5.5V, I_{OUT}=2A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=1	—	1	—	mV/V

Electrical Characteristics (continued)

$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	PFM, I_{OUT}=0A-2A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=0	—	16.5	—	mV/A
		Ultrasonic Mode, I_{OUT}=0A-2A, Address 0x04, V_{OUT} [6:0]=0x28, BB_UMODE=1, BB_FPWM=0	—	16.5	—	mV/A
		PWM, , I_{OUT}=0A-2A, Address 0x04, V_{OUT} [6:0]=0x28, MODE=1	—	3.5	—	mV/A
PG Detection	Threshold	Percentage of output regulation	75	80	85	%
	Thresholds Hysteresis	—	—	5	—	%
PG Low Voltage	PG LOW	I_{PG} Sink = 3mA	—	—	0.4	V
PG Delay	Rising Edge	—	—	1.5	—	ms
	Falling Edge	—	—	3	—	μs
V_{EN_H}, V_{MODE_H}, V_{OCP_H}	EN/MODE/OCP Logic High	—	1.4	—	—	V
V_{EN_L}, V_{MODE_L}, V_{OCP_L}	EN/MODE/OCP Logic Low	—	—	—	0.4	V
I_{EN}	EN Input Current	V_{EN} = 5.5V, EN_PD BIT = 0	—	0.1	—	μA
		V_{EN} = 0V	—	0.1	—	μA
I_{OCP}	OCP Input Current	V_{OCP} = 5.5V	—	0.1	—	μA
		V_{OCP}= 0V	—	0.1	—	μA
I_{MODE}	MODE Input Current	V_{MODE} = 5.5V	—	1	—	μA
		V_{MODE} = 0V	—	0.1	—	μA
T_{SS}	Soft-Start Period	OCP = 0V	—	0.8	—	ms
		OCP = V_{IN}	—	0.12	—	
T_{SD}	Thermal Shutdown (Note 8)	—	—	150	—	°C
	Thermal Hysteresis (Note 8)	—	—	15	—	°C
I^2C Electrical Characteristics						
V_{IO}	VI Voltage Range	—	1.7	—	5.5	V
SCL, SDA	SCL, SDA Input High Voltage Threshold	—	0.7 x V_{IO}	—	—	V
	SCL, SDA Input Low Voltage Threshold	—	—	—	0.3 x V_{IO}	V
	Hysteresis	—	—	0.05 x V_{IO}	—	V
	Input Current	—	-10	—	10	μA
	Input Capacitance	—	—	10	—	pF
SDA	Output Low Voltage	I_{SINK} = 20mA	—	—	0.4	V
t_{OF}	Output Fall Time from VIO to 0.3 × VIO	—	—	—	120	ns

Electrical Characteristics (cont.)

I^2C – Compatible Interface Timing (Standard, Fast, and Fast Mode Plus) (Note 8)						
F_{SCL}	Clock Frequency	—	—	—	—	MHz
$t_{SU;STA}$	Setup Time (Repeated) Start Condition	SCL rising edge to SDA falling edge; Both crossing High threshold	0.26	—	—	µs
$t_{HD;STA}$	Hold Time (Repeated) Start Condition	From SDA falling edge crossing Low threshold to SCL falling edge crossing High threshold	0.26	—	—	µs
t_{LOW}	SCL low period	Time measured during the Low voltage threshold	0.5	—	—	µs
t_{HIGH}	SCL high period	Time measured during the High voltage threshold	0.26	—	—	µs
$t_{HD;DAT}$	Input Data Hold Time	From SCL falling edge crossing Low threshold to SDA entering the Low-High window	0	—	—	µs
$t_{SU;DAT}$	Input Data Setup Time	From SDA exiting the Low-High window to SCL rising edge crossing Low threshold	50	—	—	ns
$t_{SU;STO}$	Setup Time for Stop Condition	From SCL rising edge crossing High threshold to SDA rising edge crossing Low threshold	0.26	—	—	µs
t_{BUF}	Bus-Free Time Between Stop and Start	From SDA crossing High threshold during STOP condition to SDA crossing High threshold for the following START condition	0.5	—	—	µs
t_{SP}	Maximum Pulse width of Spike That Must be Suppressed by the Input Filter	Any pulse width narrower than the maximum specification is suppressed	—	50	—	ns
C_B	Capacitive Load for each Bus Line	Total on-chip and off-chip capacitance	—	—	550	pF

Note: 8. All minimum and maximum parameters compliance to the datasheet limits are assured by one or more methods: production test, characterization, and/or design.

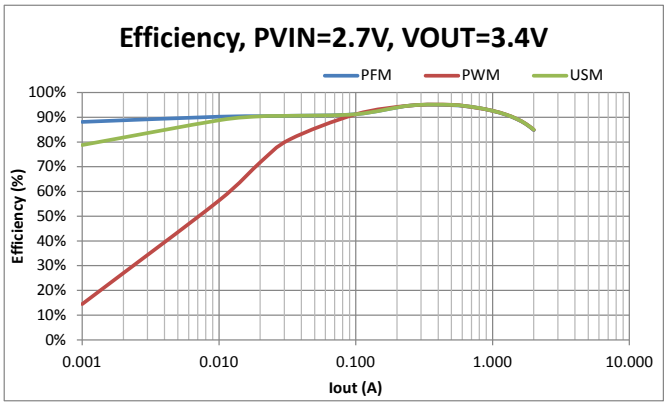
Electrical Characteristics (cont.)

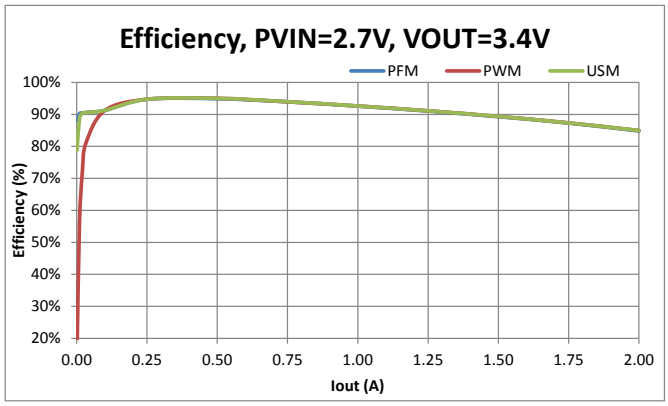
I^2C – Compatible Interface Timing (High-speed Mode, C_B=100pF) (Note 8)						
F_{SCL}	Clock Frequency	—	—	—	3.4	MHz
$t_{SU;STA}$	Setup Time (Repeated) Start Condition	SCL rising edge to SDA falling edge; Both crossing High threshold	160	—	—	ns
$t_{HD;STA}$	Hold Time (Repeated) Start Condition	From SDA falling edge crossing Low threshold to SCL falling edge crossing High threshold	160	—	—	ns
t_{LOW}	SCL low period	Time measured during the Low voltage threshold	160	—	—	ns
t_{HIGH}	SCL high period	Time measured during the High voltage threshold	60	—	—	ns
$t_{HD;DAT}$	Input Data Hold Time	From SCL falling edge crossing Low threshold to SDA entering the Low-High window	—	35	—	ns
$t_{SU;DAT}$	Input Data Setup Time	From SDA exiting the Low-High window to SCL rising edge crossing Low threshold	10	—	—	ns
$t_{SU;STO}$	Setup Time for Stop Condition	From SCL rising edge crossing High threshold to SDA rising edge crossing Low threshold	160	—	—	ns
t_{RCL}	SCL rise time	—	10	—	40	ns
t_{RCL1}	Rise time of SCL signal after REPEATED START condition and after Acknowledge bit	—	10	—	80	ns
t_{FCL}	SCL fall time	—	10	—	40	ns
t_{RDA}	SDA rise time	—	—	—	80	ns
t_{FDA}	SDA fall time	—	—	—	80	ns
t_{BUF}	Bus-Free Time Between Stop and Start	From SDA crossing High threshold during STOP condition to SDA crossing High threshold for the following START condition	—	10	—	ns
t_{SP}	Maximum Pulse width of Spike That Must be Suppressed by the Input Filter	Any pulse width narrower than the maximum specification is suppressed	—	10	—	ns
C_B	Capacitive Load for each Bus Line	Total on-chip and off-chip	—	—	100	pF

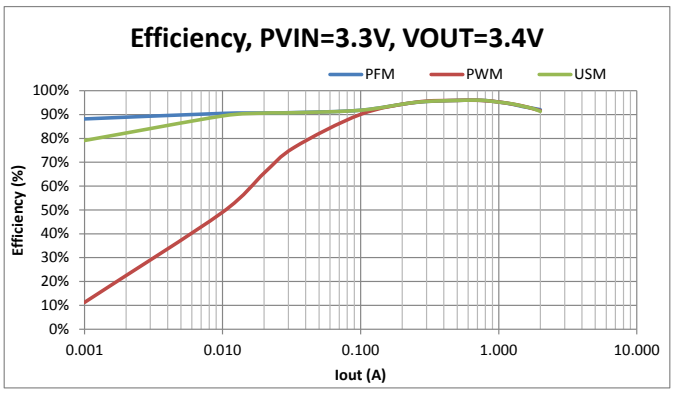
Note: 8. All minimum and maximum parameters compliance to the datasheet limits are assured by one or more methods: production test, characterization, and/or design.

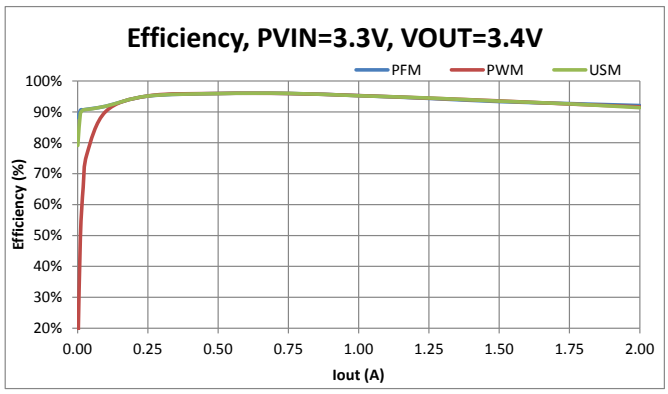
Typical Performance Characteristics

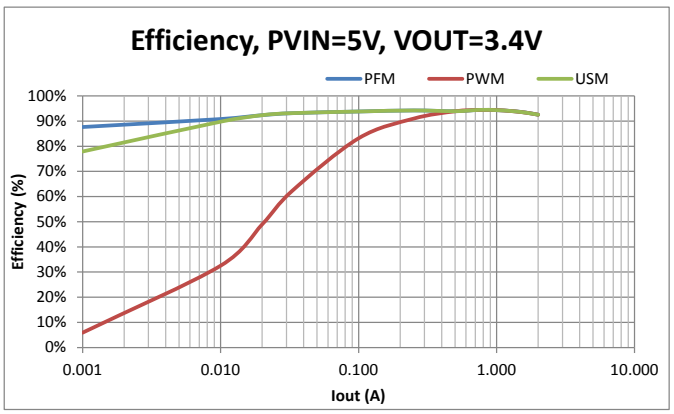
(@T_A = +25°C, PV_{IN} = V_{IN} = V_{IO} = 2.3V to 5.5V, V_{OUT} = 3.4V, L = 1µH, unless otherwise specified.)

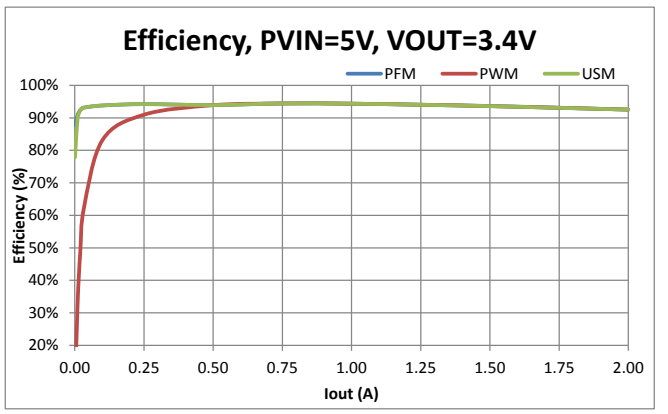


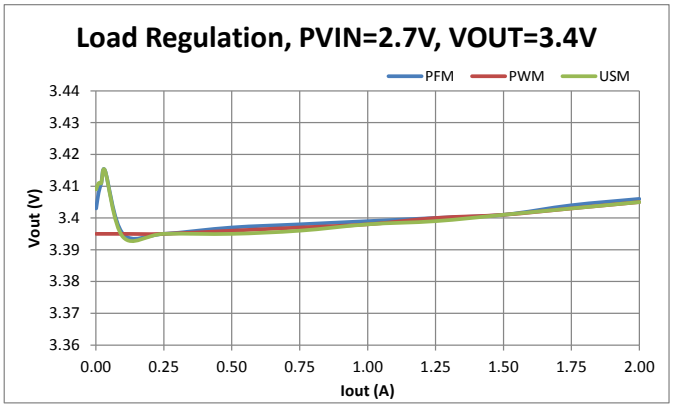


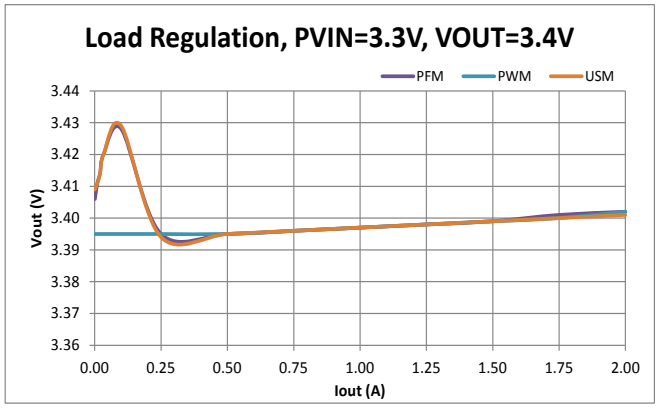












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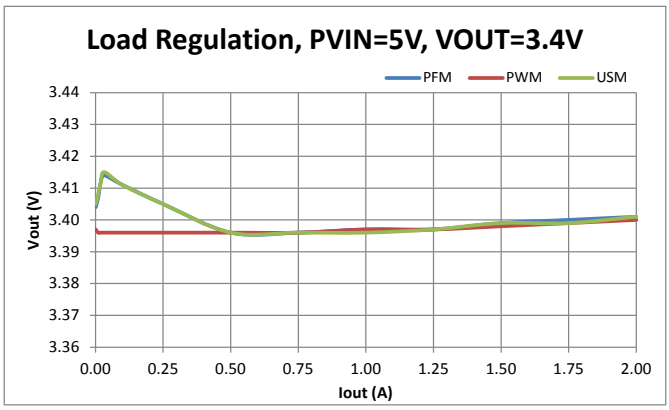

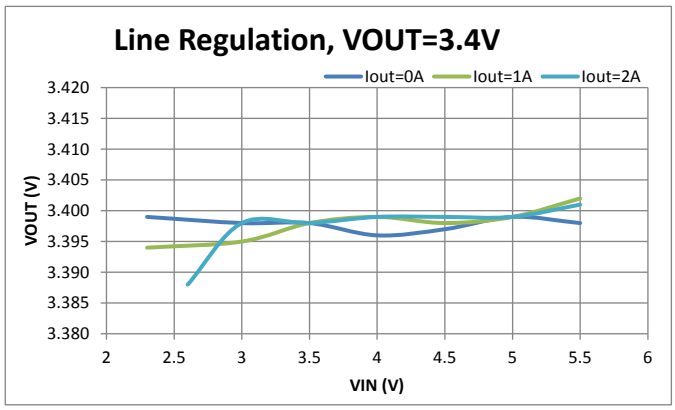

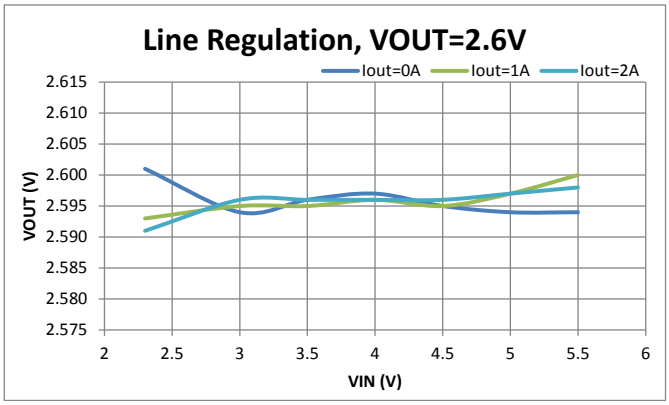

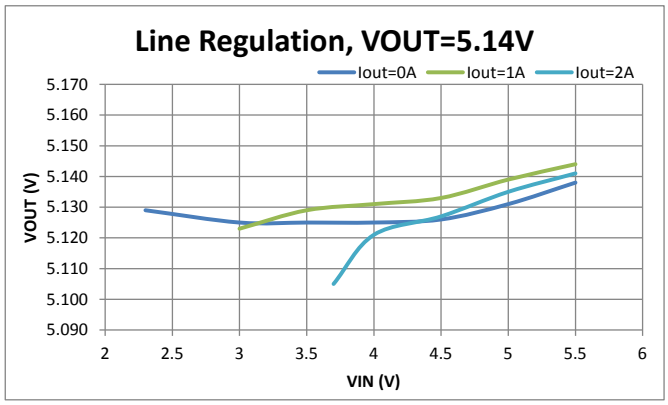

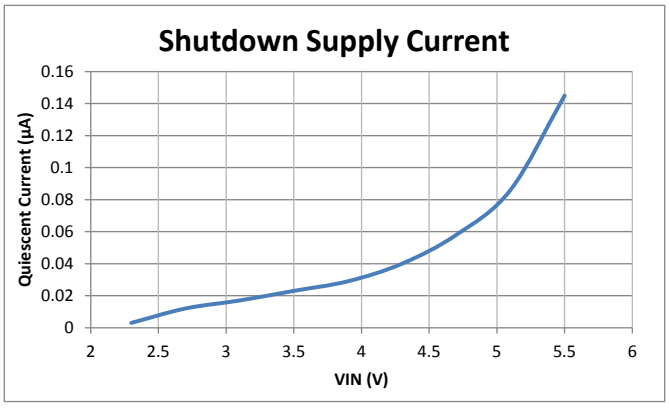

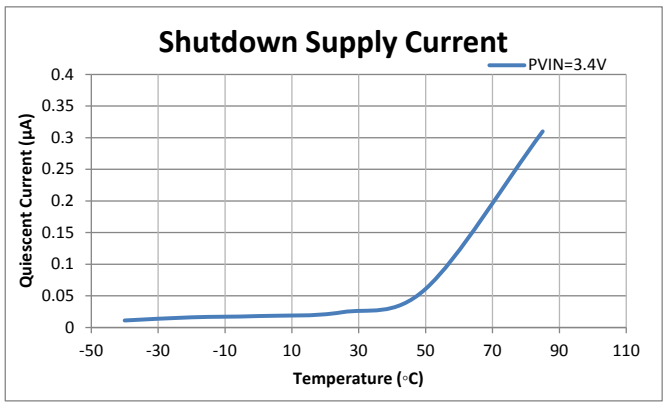

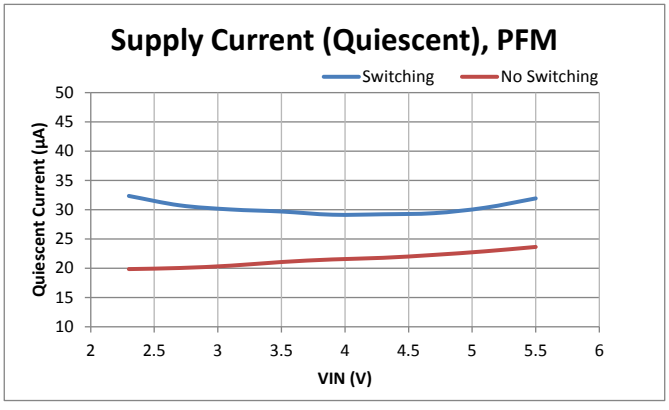

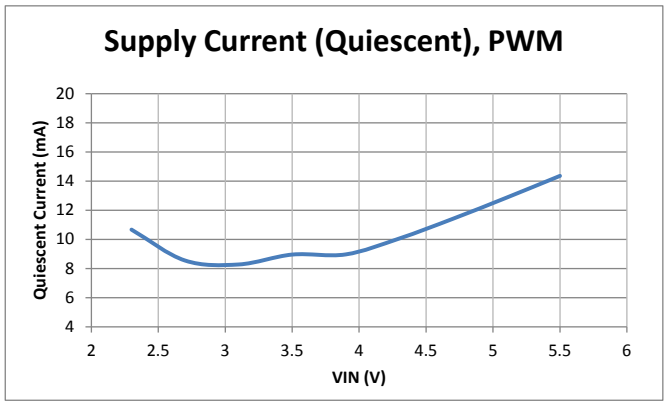

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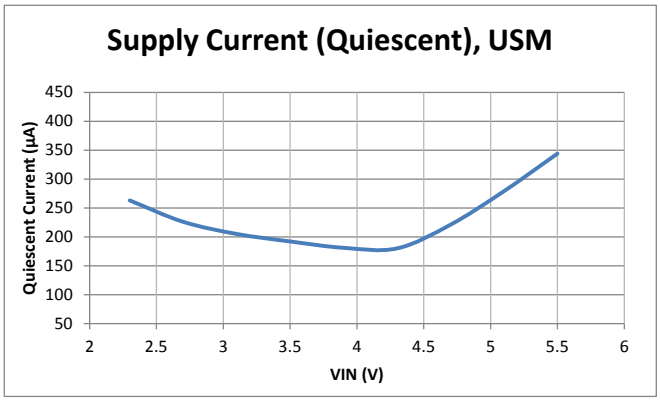
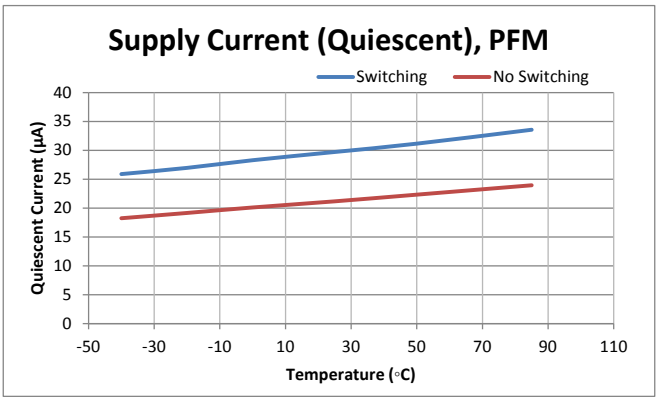
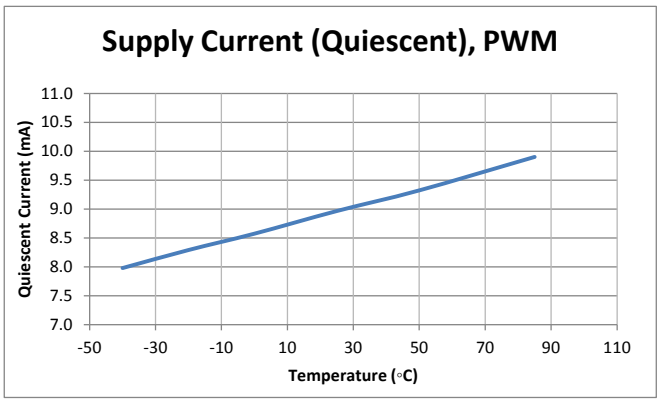
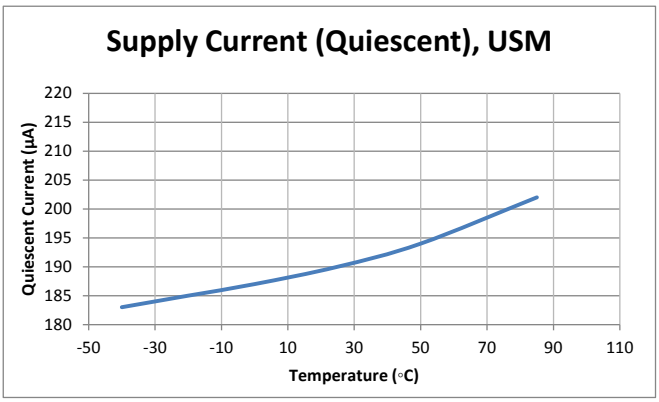
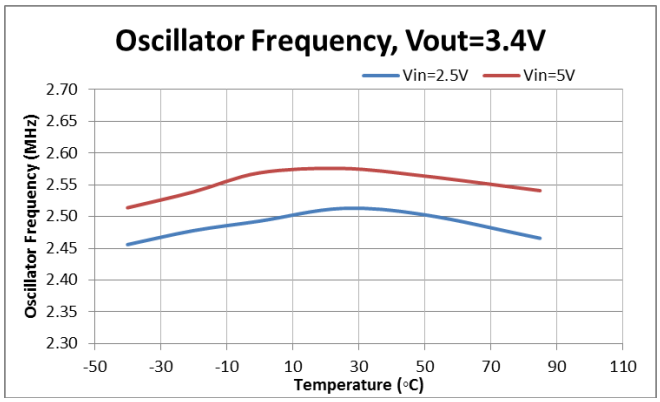
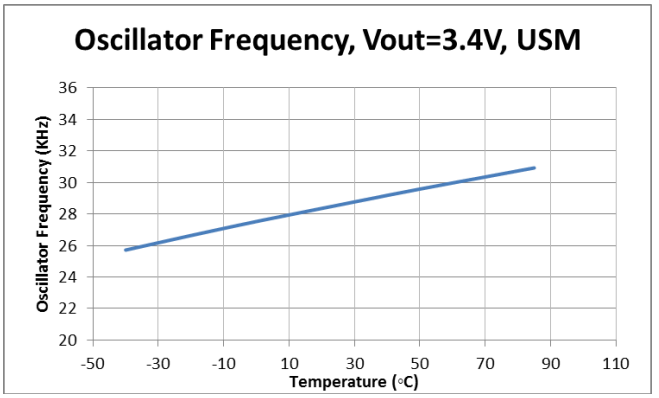








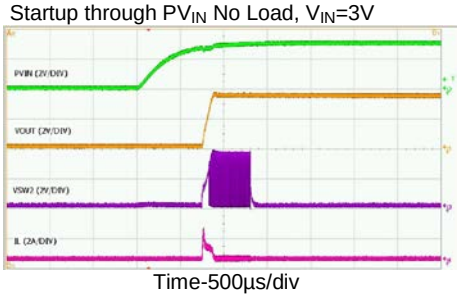




Typical Performance Characteristics (Continued)

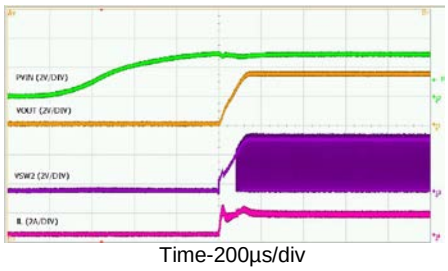
(@T_A = +25°C, PV_{IN} = V_{IN} = V_{IO} = 2.3V to 5.5V, V_{OUT} = 3.4V, L = 1µH, unless otherwise specified.)

Startup through PV_{IN} No Load, V_{IN}=3V



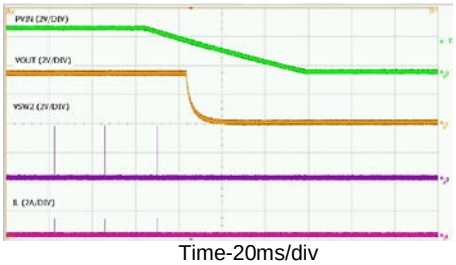
Time-500µs/div

Startup through PV_{IN} 1A Load, V_{IN}=3V



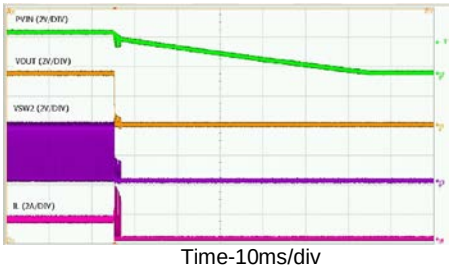
Time-200µs/div

Shutdown through PV_{IN} No Load, V_{IN}=3V



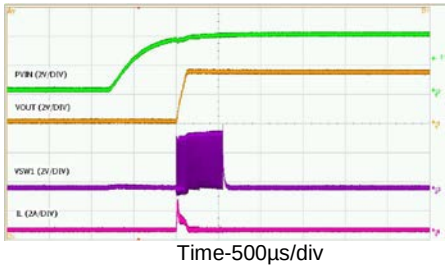
Time-20ms/div

Shutdown through PV_{IN} 1A Load, V_{IN}=3V



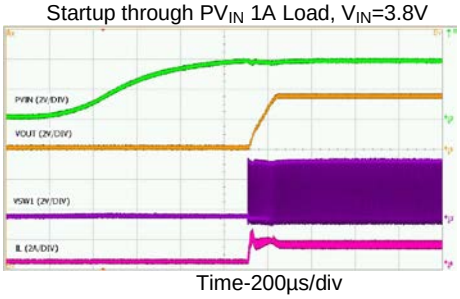
Time-10ms/div

Startup through PV_{IN} No Load, V_{IN}=3.8V



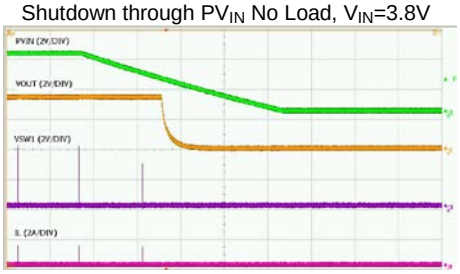
Time-500µs/div

Startup through PV_{IN} 1A Load, V_{IN}=3.8V



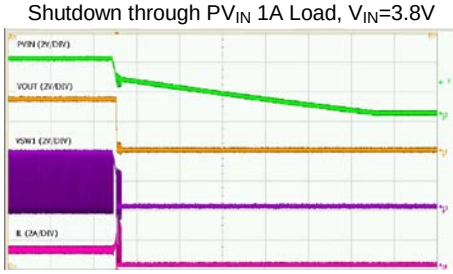
Time-200µs/div

Shutdown through PV_{IN} No Load, V_{IN}=3.8V



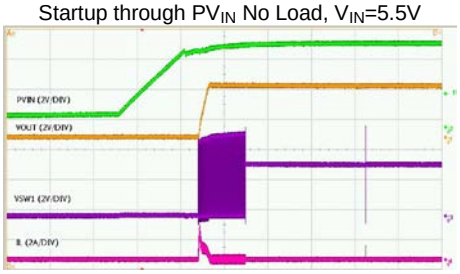
Time-20ms/div

Shutdown through PV_{IN} 1A Load, V_{IN}=3.8V



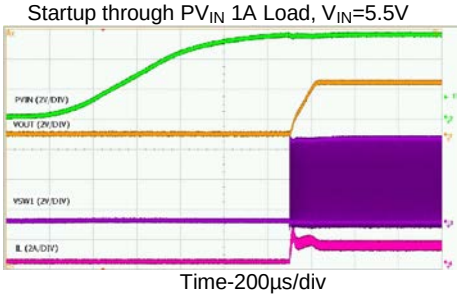
Time-10ms/div

Startup through PV_{IN} No Load, V_{IN}=5.5V



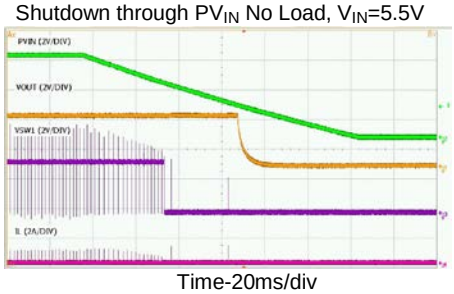
Time-500µs/div

Startup through PV_{IN} 1A Load, V_{IN}=5.5V



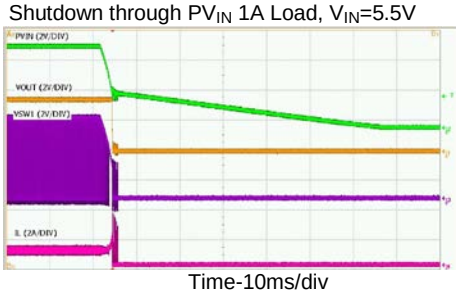
Time-200µs/div

Shutdown through PV_{IN} No Load, V_{IN}=5.5V



Time-20ms/div

Shutdown through PV_{IN} 1A Load, V_{IN}=5.5V

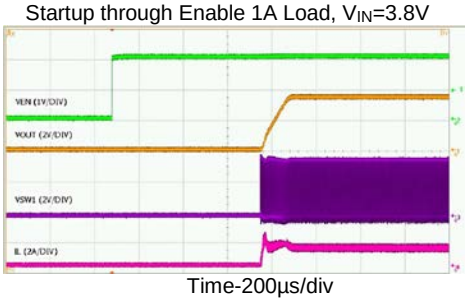


Time-10ms/div

Startup through Enable No Load, V_{IN}=3.8V

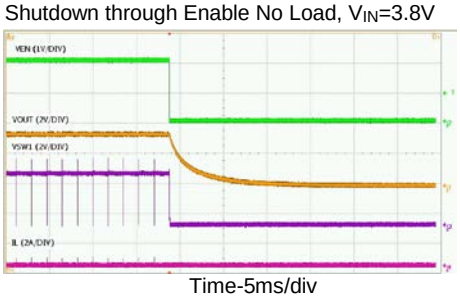
Time-200µs/div

Startup through Enable 1A Load, V_{IN}=3.8V



Time-200µs/div

Shutdown through Enable No Load, V_{IN}=3.8V

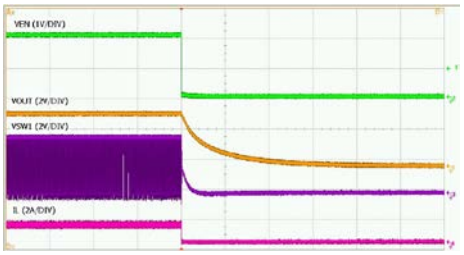


Time-5ms/div

Typical Performance Characteristics (Cont.)

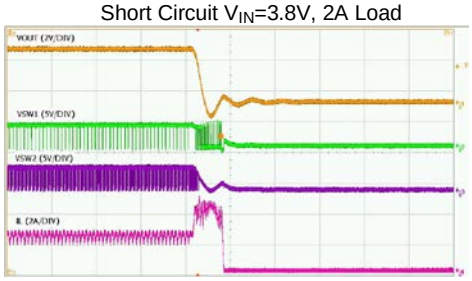
(@T_A = +25°C, PV_{IN} = V_{IN} = V_{IO} = 2.3V to 5.5V, V_{OUT} = 3.4V, L = 1µH, unless otherwise specified.)

Shutdown through Enable 1A Load, V_{IN}=3.8V



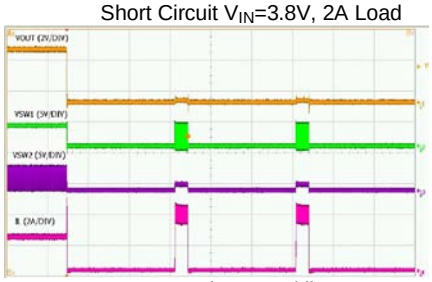
Time-100µs/div

Short Circuit V_{IN}=3.8V, 2A Load



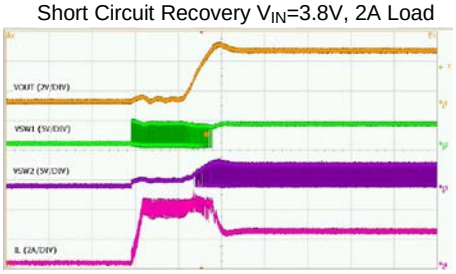
Time-50µs/div

Short Circuit V_{IN}=3.8V, 2A Load



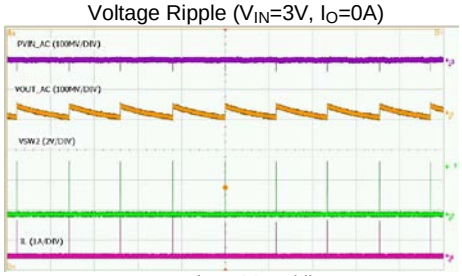
Time-5ms/div

Short Circuit Recovery V_{IN}=3.8V, 2A Load



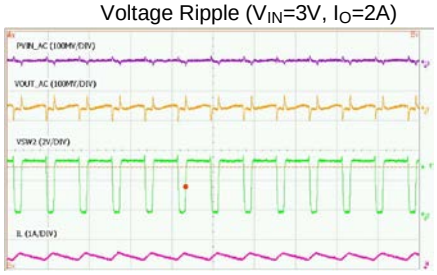
Time-100µs/div

Voltage Ripple (V_{IN}=3V, I_O=0A)



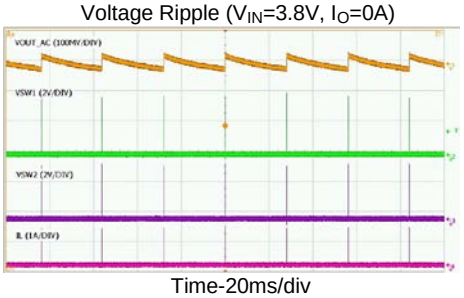
Time-20ms/div

Voltage Ripple (V_{IN}=3V, I_O=2A)



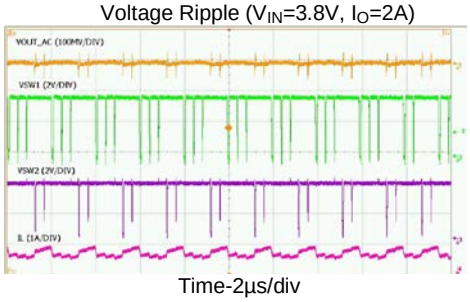
Time-500ns/div

Voltage Ripple (V_{IN}=3.8V, I_O=0A)



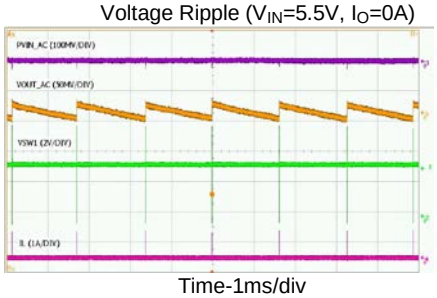
Time-20ms/div

Voltage Ripple (V_{IN}=3.8V, I_O=2A)



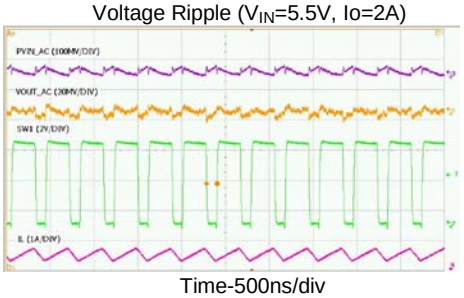
Time-2µs/div

Voltage Ripple (V_{IN}=5.5V, I_O=0A)



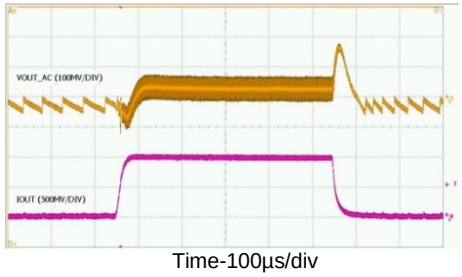
Time-1ms/div

Voltage Ripple (V_{IN}=5.5V, Io=2A)



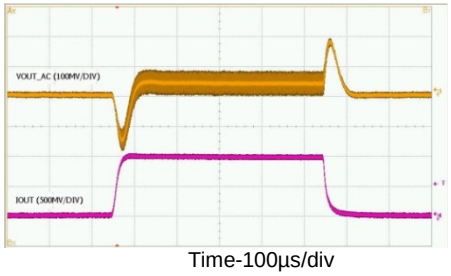
Time-500ns/div

Load Transient (V_{IN}=3V, PFM, I_O=0A to 1A)



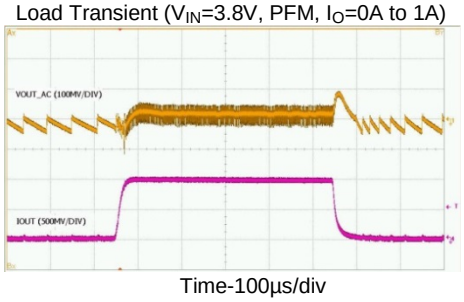
Time-100µs/div

Load Transient (V_{IN}=3V, PWM, I_O=0A to 1A)



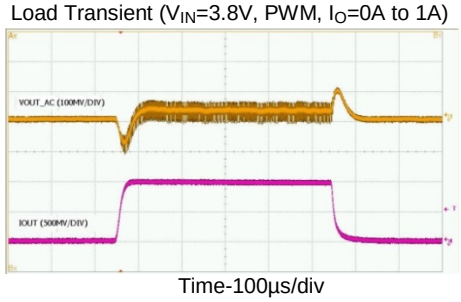
Time-100µs/div

Load Transient (V_{IN}=3.8V, PFM, I_O=0A to 1A)



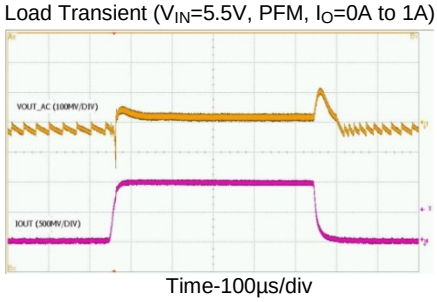
Time-100µs/div

Load Transient (V_{IN}=3.8V, PWM, I_O=0A to 1A)



Time-100µs/div

Load Transient (V_{IN}=5.5V, PFM, I_O=0A to 1A)

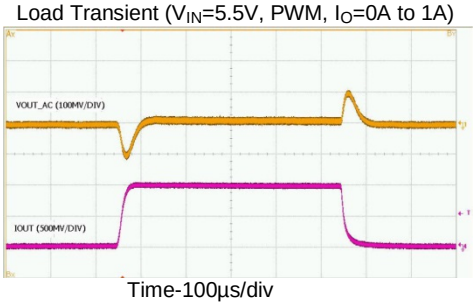


Time-100µs/div

Typical Performance Characteristics (Cont.)

(@T_A = +25°C, PV_{IN} = V_{IN} = V_{IO} = 2.3V to 5.5V, V_{OUT} = 3.4V, L = 1µH, unless otherwise specified.)

Load Transient (V_{IN}=5.5V, PWM, I_O=0A to 1A)



Time-100µs/div

Application Information

Buck-Boost Power Conversion

When the EN pin goes high, the AP72200 turns on the internal logic circuitries. Once VIN is supplied, all user registers are accessible through I^2C. When EN is pulled low, the AP72200 enters shutdown mode. This event resets all registers to their default values. The AP72200 can operate in either buck or boost mode. Refer to the functional block diagram. When the input voltage PVIN is less than output VOUT, Q1 will be on continuously while Q2 remains off. Q3 and Q4 switch to boost the output up. When the input voltage PVIN is more than output VOUT, Q3 will be on continuously while Q4 remains off. Q1 and Q2 switch to buck the output down. In the event when operating in conditions where PVIN is close to VOUT, the AP72200 alternates between buck and boost mode as necessary to provide a regulated output voltage.

Regulator Enable Control

Buck-boost has an enable pin EN as well as I^2C enable bit. As shown in Table 1 below, the AP72200 turns on the internal bias circuitry when EN pin goes high. Once VIO is supplied, all the user registers are accessible through I^2C. The address register 0x03 bit 6 is the BB_EN. Changing this bit to 0 will disable the output voltage while the internal logic circuitries are still active. Pulling EN low will turn off the AP72200 and reset all registers to their POR default values.

EN	BB_EN BIT	Operating Condition
LOW	x	Device OFF
HIGH	0	Disable Output
HIGH	1 (Default)	Enable Output

Table 1 Enable Control Logic Truth Table

H-Bridge Controller

H-bridge architecture operates at 2.5MHz fixed frequency with a pulse width modulated (PWM), current-mode control scheme. This topology is in a cascade of a boost regulator and a buck regulator using a single inductor and output capacitor. Buck, buck-boost, and boost stages are 100% synchronous for highest efficiency in portable applications. Figure 2 shows a simplified diagram of the internal switches, external inductor, and output capacitor.

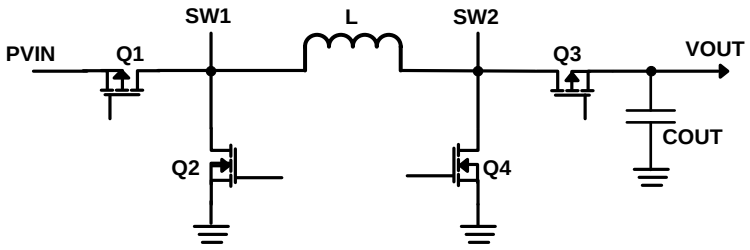


Figure 2 Buck-Boost Diagram

In buck PWM, Switch Q3 is continuously closed and Switch Q4 is continuously open. Switches Q1 and Q2 operate as a synchronous buck converter when in this condition. In boost PWM, Switch Q1 remains closed and Switch Q2 remains open. Switches Q3 and Q4 operate as a synchronous boost converter when in this operation. When the input voltage is dropping close to the output voltage such that the duty cycle seen at SW1 is more than 90%, then the regulator will switch from buck to buck-boost (where cycles will alternate between buck and boost). The AP72200 will rapidly and smoothly switch from boost-to-buck mode as needed to maintain the regulated output voltage. As the input voltage continues to drop such that the duty cycle in boost mode is more than 10% seen at SW2, then the regulator switches to all boost operation. This behavior provides excellent efficiency and very low output voltage ripple.

Application Information (continued)

H-Bridge Controller (continued)

The regulator enters PFM as the output load decrease when the valley of the inductor current is less than 0A. The zero cross detection will activate after 40µs delay before switching the mode from PWM to PFM. During PFM operation in buck mode, Switch Q3 is closed and Switch Q4 is open. Switches Q1 and Q2 operate in discontinuous mode during PFM operation until output voltage is approximately 1.2% upper threshold of the PFM hysteretic controller. Then all switches are open to allow VOUT to decay until it reaches nominal regulation before switching again. This operation will reduce switching losses at light load thus improving efficiency. Likewise, the AP72200 closes Switch Q1 and Switch Q4 to ramp up the current in the inductor during PFM operation in boost mode. When the inductor current reaches 1A, the device turned OFF Switch Q4, then turn ON Switch Q3. With Switch Q3 closed, output voltage increases as the inductor current ramps down. When the loading current gets higher, there will be multiple PFM pulses to charge up the output capacitor. These pulses continue until VOUT has achieved the 1.2% upper threshold of the PFM hysteretic controller. Switching action then stops until VOUT decays until it reached normal regulation before switching again. The regulator resumes normal PWM operation as the output load increases and VOUT drops 2% below the regulation point.

Regulator MODE Control

AP72200 has a MODE pin as well as I^2C enable bit. Connect MODE pin low sets the regulator to operate in PFM. Tie the MODE to VIN set the device in PWM. The MODE pin condition is set during the POR operation of the regulator and can only be overridden by the I^2C. In the address number 0x02, bit 6 and bit 0 are BB_UMODE and BB_FPWM respectively. These two bits can set the mode of operation of PFM, enhanced ultrasonic, or forced PWM.

When the enhanced ultrasonic is set, this activates a unique pulse-skipping mode with a minimum switching frequency of 20kHz. An ultrasonic pulse occurs when the regulator detects that no switching has occurred after 37µs. Once triggered, the ultrasonic pulse turned on the switch Q2 (buck mode) or Q3 (boost mode) for approximately 50ns to induce a negative inductor current. This process continues until FB drops to the regulation point. Then the regulator waits for the next clock edge to initiate the ON time. Table 2 is the truth table for the MODE operation found in I^2C address 0x02.

BIT6	BIT0	Operating Mode
0	0	PFM
1	0	Ultrasonic Mode
x	1	PWM

Table 2 MODE Control Table

Power-Good (PG) Indicator

Buck-boost has an open-drain output that is actively held low during soft-start period until the output voltage reaches 80%. When the output voltage is outside of its regulation by -20%, the PG will pull low until the output returns to set value. The PG low-to-high transition is delayed by 1.5ms while the falling edge PG is delayed by 3µs to prevent false triggering. The polarity of PG output is programmable through I^2C in address 0x03 bit 4. It is active high by default.

Overcurrent Protection

AP72200 has an OCP pin as well as an I^2C enable bit to adjust the threshold 2A or 4.3A. The OCP pin control setting is the condition upon POR operation of the regulator and can only be overridden by the I^2C. The AP72200 detects the current limit on the high side, Q1, to protect the device against overload or short-circuit conditions. The peak current in the switch is monitored cycle by cycle with comparator delay approximately 100ns to guard against noise glitches. If the high-side Q1 current limit is reached, the high-side Q1 is turned off, and the low-side Q2 is turned on until the switch current decreases below OC threshold. The frequency is reduced in order to protect the device from damage. The Q1 peak current limit remains active during this state. After 17 consecutive cycles in OCP event, the regulator enters hiccup mode where all power FETs turn off and wait for 15ms before attempting to restart.

Reverse Current Protection

During fixed-frequency operation, a reverse-current comparator on switch Q2 monitors the current entering VOUT. When this current exceeds 2A (typical), switch Q2 will be turned off for the remainder of the switching cycle. This feature protects the buck-boost converter from excessive reverse current if the buck-boost output is held above the regulation voltage by an external source.

Undervoltage Lockout

The undervoltage lockout (UVLO) feature prevents abnormal operation in the event that the supply voltage is too low to guarantee proper operation. When the VIN voltage falls below the UVLO threshold, the regulator is disabled.

Application Information (cont.)

Thermal Shutdown

A built-in thermal protection feature protects the AP72200 if the die temperature reaches +150°C (typical). At this die temperature, the regulator is completely shut down. The die temperature continues to be monitored in this thermal-shutdown mode. When the die temperature falls to +135°C (typical), the device will resume normal operation. When exiting thermal shutdown, the AP72200 will execute its soft-start sequence.

Output Voltage Slew-rate Control

Buck-boost regulator supports programmable slew-rate control feature when increasing and decreasing the output voltage. The ramp-up slew-rate can be set to 20mV/µs or 40mV/µs through BB_RU_SR bit, and the ramp-down slew-rate is programmable to 5mV/µs or 10mV/µs through BB_RD_SR bit in I^2C address 0x02.

Output Active Discharge

AP72200 provides an internal 100Ω resistor for output active discharge function. If the active discharge function is enabled (BB_AD = 1 in I^2C address 0x02), the internal resistor discharges the energy stored in the output capacitor to PGND whenever the regulator is disabled. Either the regulator remains enabled or the active discharge function is disabled (BB_AD = 0), the internal resistor is disconnected from the output. If the active discharge function is disabled, the output voltage decays at a rate that is determined by the output capacitance and the load current when the regulator is turned off.

Inductor Selection

An inductor with high-frequency core material (e.g., ferrite core) should be used to minimize core losses and provide good efficiency. The inductor must be able to handle the peak switching currents without saturating. A 1µH inductor with ≥4.4A saturation current rating is recommended. Select an inductor with low DCR to provide good efficiency. In applications where radiated noise must be minimized, a toroidal or shielded inductor can be used.

PVIN and VOUT Capacitor Selection

The input and output capacitors should be ceramic X5R type with low ESL and ESR. The recommended input capacitor value is 22µF, as this would provide adequate RMS current to minimize the input voltage ripple. A minimum of 10µF is required to maintain full functionality of the part. The recommended output capacitor is 2x22µF, 10V, X5R. Note that the effective value of a ceramic capacitor derates with DC voltage bias across it. This derating may be up to 70% of the rated capacitance. Refer to the capacitor datasheet to ensure the combined effective output capacitance is at least 30µF for proper operation over the entire recommended load current range. Low-output capacitance may lead to large output voltage drop during load transient or unstable operation.

Serial Interface

The I²C compatible 2-wire serial interface is used for regulator on/off control, setting output voltages, and other functions. See the Register Map section for details. The I²C interface is an open-drain serial bus that consists of a bidirectional serial data line (SDA) and a serial clock line (SCL). Pull-up resistors of 500Ω each or greater must be added from VIO to SDA and VIO to SCL. Optional 24Ω resistors in series with SDA and SCL help protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

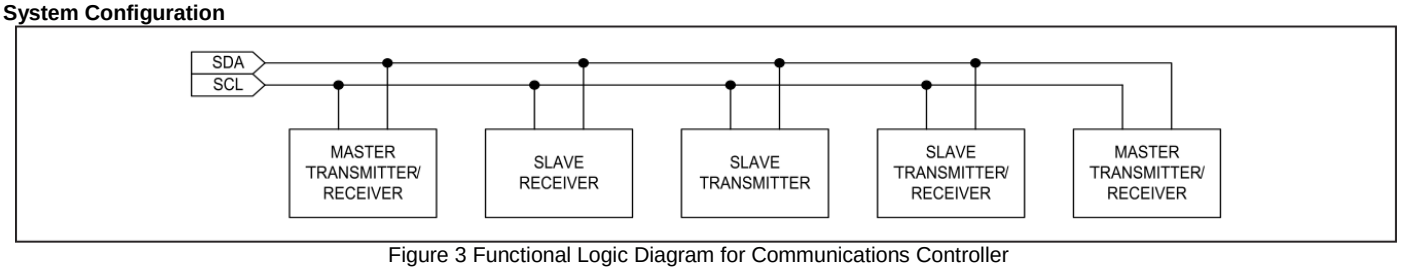


Figure 3 Functional Logic Diagram for Communications Controller

The I²C bus is a multi-master bus. The maximum number of devices that can attach to the bus is limited by bus capacitance. Figure 3 shows an example of a typical I²C system. A transmitter is a device on the I²C bus that sends data to the bus. A receiver is a device that receives data from the bus. The master is a device that initiates a data transfer and generates the SCL clock signal to control the data transfer. A slave is any device on the bus that can be addressed by the master. When the AP72200 I²C compatible interface is operating, it is a slave on I²C bus.

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

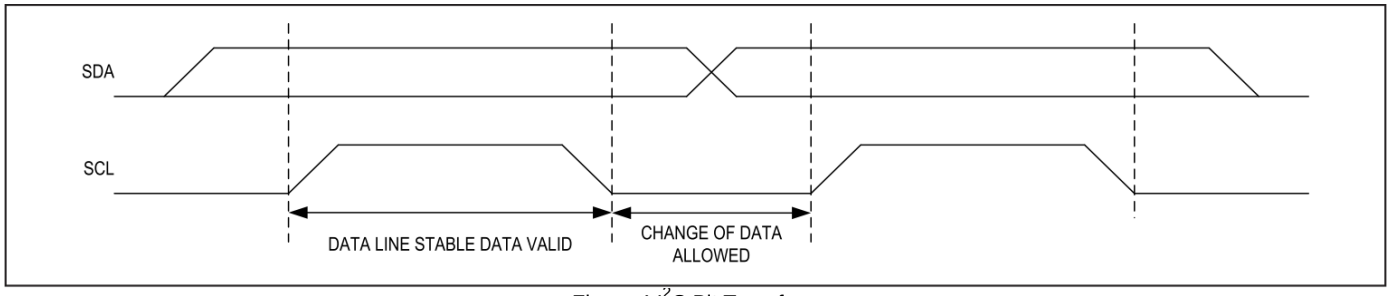


Figure 4 I²C Bit Transfer

START and STOP Conditions

When the I²C serial interface is inactive, SDA and SCL are pulled high. A master device initiates communication by issuing a START (S) condition. A START condition is a high-to-low transition on SDA while SCL is high. A STOP (P) condition is a low-to-high transition on SDA while SCL is high. A START condition from the master signals the AP72200 that a transmission is about to begin. The master terminates transmission and frees the bus by issuing a STOP condition. To issue a series of commands to the slave, the master may issue REPEATED START (Sr) conditions instead of a STOP condition in order to maintain control of the bus. In general, a REPEATED START condition is functionally equivalent to a regular START condition. AP72200 will listen for its address after a START condition is detected. If its address is not detected, it will stay idle until the next START condition is detected.

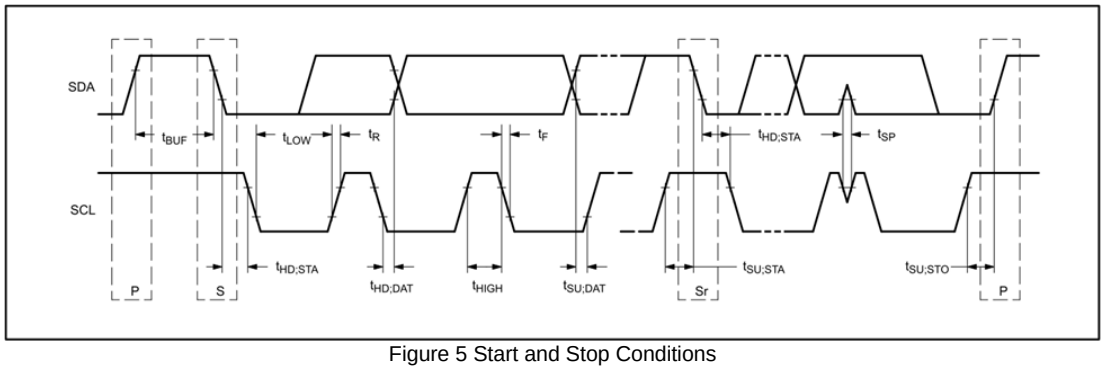


Figure 5 Start and Stop Conditions

Acknowledge

Both I²C bus master and AP72200 (slave) generate ACKNOWLEDGE (ACK) bits when receiving data. The ACK bit is the last bit of each nine bit data packet. To generate an ACK bit, the receiving device must pull SDA low before the rising edge of the ACK-related clock pulse (ninth SCL pulse) and keep it low during the high period of the clock pulse. To generate a NOT ACKNOWLEDGE (nACK), the receiving device allows SDA to be pulled high before the rising edge of the ACK-related clock pulse and leaves it high during the high period of the clock pulse. Monitoring the ACK bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The I²C slave address of the AP72200 is shown in table below:

Slave Address (7 Bit)	Slave Address (Write)	Slave Address (Read)
100 0011	0x86 (1000 0110)	0x87 (1000 0111)

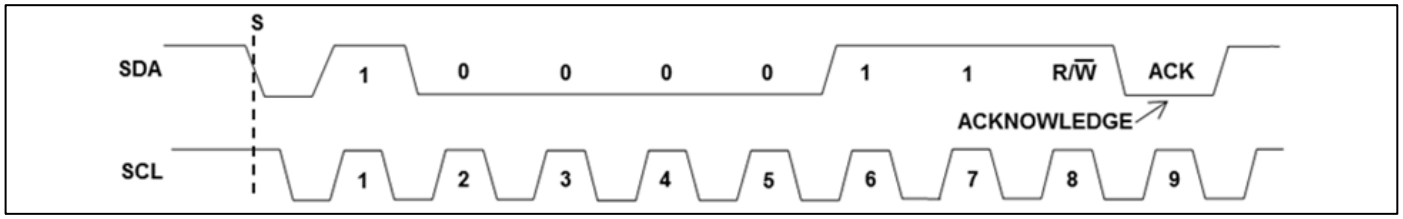


Figure 6 Slave Address Byte Example

Clock Stretching

In general, the clock signal generation for the I²C bus is the responsibility of the master device. I²C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The AP72200 does not use any form of clock stretching to hold down the clock line.

General Call Address

The AP72200 does not implement the I²C specification called general call address. If the AP72200 sees a general call address (00000000b), it does not issue an ACKNOWLEDGE.

Communication Speed

The AP72200 provides I²C 3.0-compatible serial interface.

- I²C revision 3-compatible serial communications channel
  - 0Hz to 100kHz (Standard-mode)
  - 0Hz to 400kHz (Fast-mode)
  - 0Hz to 1MHz (Fast-mode Plus)
  - 0Hz to 3.4MHz (High-Speed mode)
  - Does not utilize I²C clock stretching

Operating in Standard-mode, Fast-mode, or Fast-mode Plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pull-up resistors. Higher time constants created by the bus capacitance and pull-up resistance (C × R) slow the bus operation. Therefore, when increasing bus speeds, the pull-up resistance must be decreased to maintain a reasonable time constant. Refer to the Pull-up Resistor Sizing section of I²C revision 3.0 specification for detailed guidance on the pull-up resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs pull-up resistors of 5.6kΩ, a 400kHz bus needs about a 1.5kΩ pull-up resistors, and a 1MHz bus needs 680Ω pull-up resistors. Note that the pull-up resistor is dissipating power when the open-drain bus is low. Lower values of the pull-up resistors result in higher power dissipation (V^2/R).

Operating in High-Speed (HS) mode requires some special considerations. For the full list of considerations, refer to the I2C 3.0 specification. The major considerations with respect to the AP72200 are:

- The I²C bus master uses current source pull-ups to shorten the signal rise times.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the High-Speed master code.

At power-up or after each STOP condition, the AP72200 inputs filters are set for Standard-mode, Fast-mode, or Fast-mode Plus (i.e. 0Hz to 1MHz). Use the High-Speed master code protocols that are described in Communication Protocols section to switch the input filters for High-Speed mode.

Communication Protocols

The AP72200 supports both writing and reading from its registers. The following sections show the I^2C communication protocols.

Writing to a Single Register

Figure 7 below shows the protocol for I^2C master device to write one byte of data to the AP72200 the write byte protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte.
8. The next falling edge of SCL loads the data byte into its target register and the data becomes active.
9. The master sends a STOP condition or a REPEATED START condition.

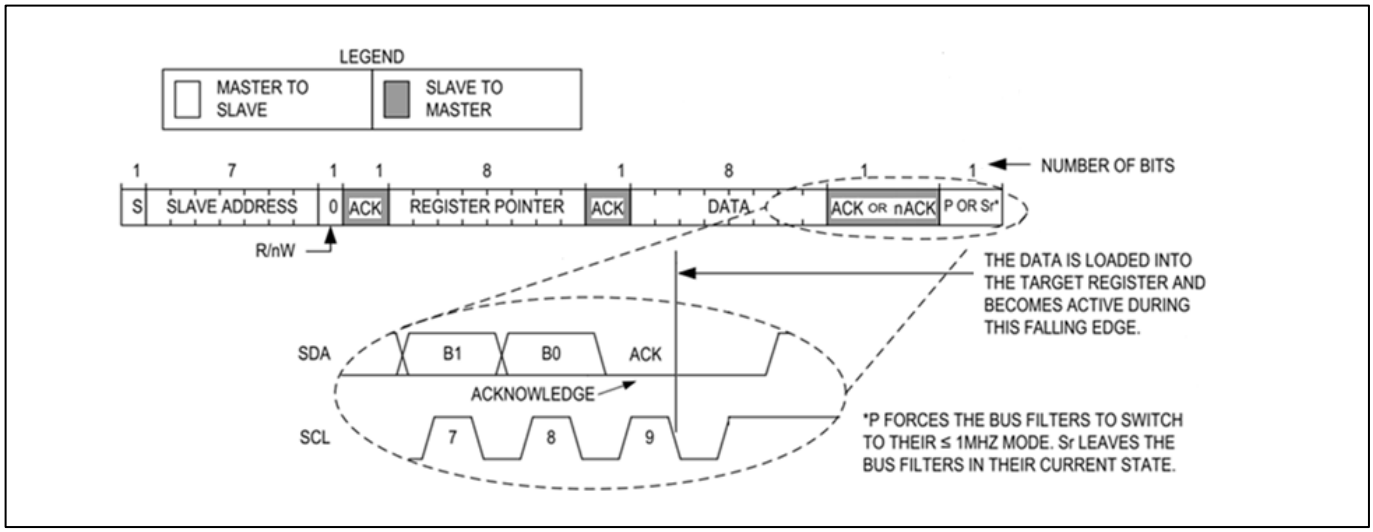


Figure 7 Writing to a Single Register with Write Byte Protocol

Writing to a Sequential Register

Figure 8 below shows the protocol for writing to sequential registers. This protocol is similar to the write byte protocol, except the master continues to write additional data after is receives an ACK from the slave that it successfully received the previous data byte. The slave's register pointer will auto-increment by one after each byte received. When the master is done writing, it issues a STOP or REPEATED START. The writing to sequential registers protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte.
8. The next falling edge on SCL loads the data byte into its target register and the data becomes active.
9. Steps 6 to 8 are repeated as many times as the master requires.
10. The master sends a STOP condition or a REPEATED START condition.

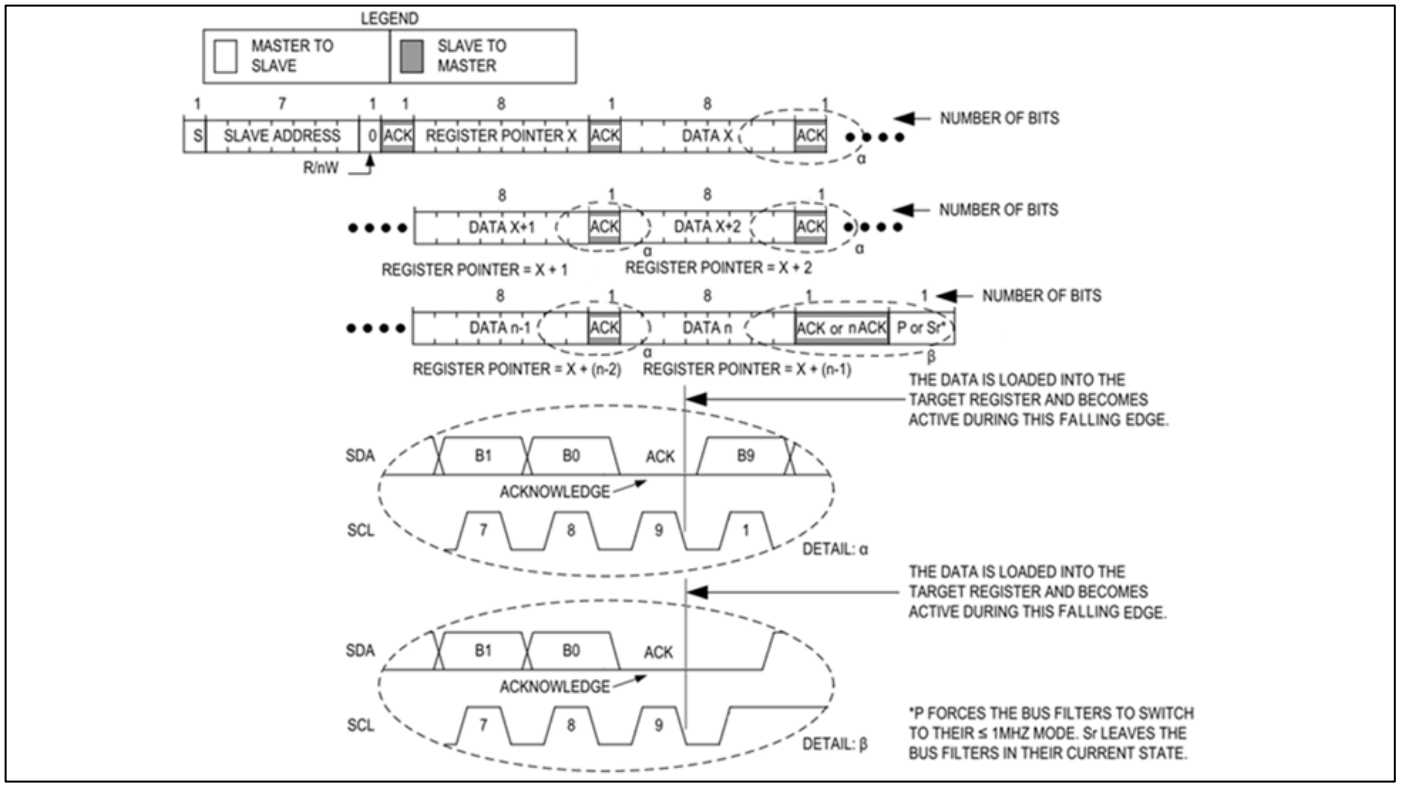


Figure 8 Writing to Sequential Registers X to N

Reading from a Single Register

The I²C master device reads one byte of data from AP72200. The read byte protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave sends an ACK bit by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the register specified by the register pointer.
10. The master issues a nACK.
11. The master sends a STOP condition or a REPEATED START condition.

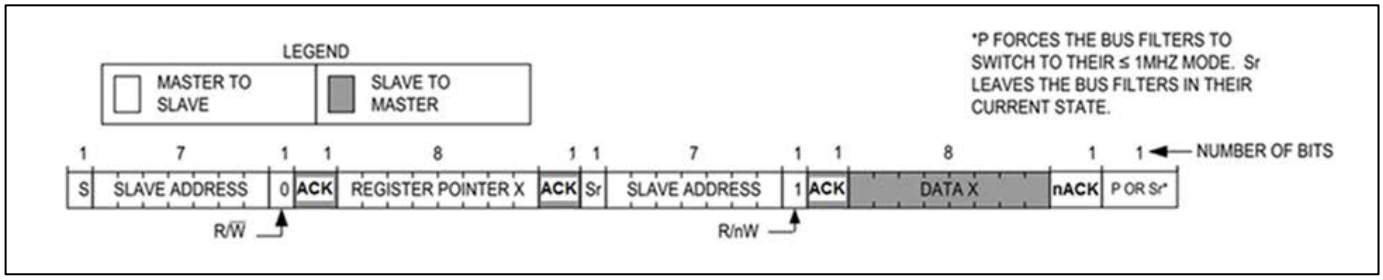


Figure 9 Reading from a Single Register X

Reading from a Sequential Register

Figure 9 below shows the protocol for reading from sequential registers. This protocol is similar to the read byte protocol except the master issues an ACK to signal the slave that it wants more data. The slave's register pointer will auto-increment by one after each byte sent. When the master has all the data it requires, it issues a nACK and a STOP to end the transmission. The continuous read from sequential registers protocol is as follows:

1. The master sends a START condition.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave sends an ACK bit pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START condition.
7. The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8. The addressed slave sends an ACK bit by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the register specified by the register pointer.
10. The master issues an ACK signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires.
12. Following the last byte of data, the master must issue a nACK to signal that it wishes to stop receiving data.
13. The master sends a STOP condition or a REPEATED START condition.

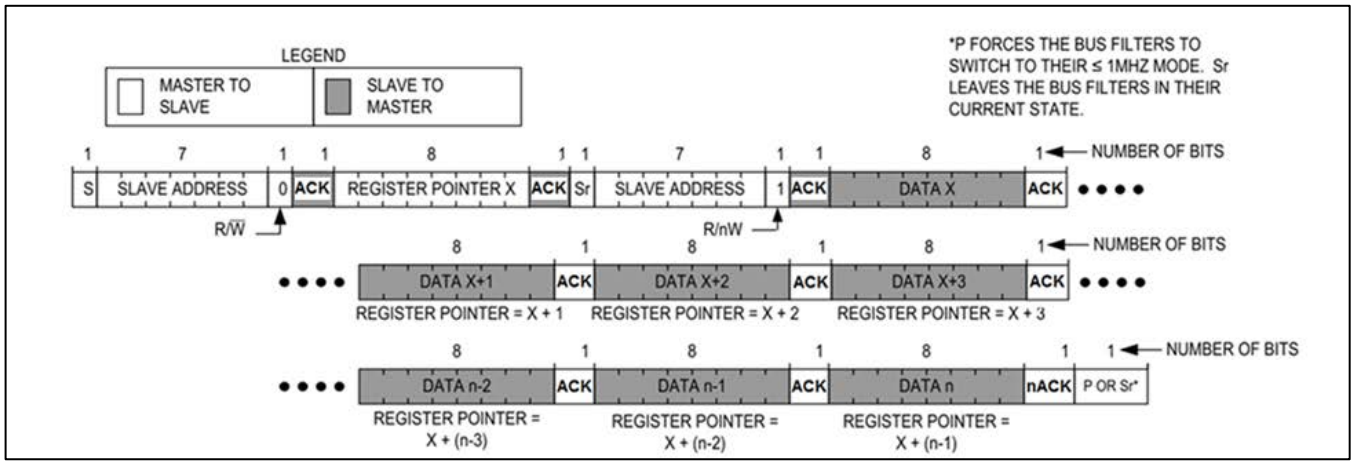


Figure 10 Reading Continuously from Sequential Registers X to N

Engaging HS Mode for Operation Up to 3.4MHz

Figure 10 below shows the protocol for engaging HS mode operation. HS mode operation allows for a bus operating speed of up to 3.4MHz. The protocol to engage HS mode is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START condition.
3. The master sends the 8-bit master code of 00001xxxb where xxxb are don't care bits.
4. The master code is not acknowledged.
4. The master switches to High-Speed communication and can now increase its bus speed up to 3.4MHZ.
5. The master sends a REPEATED START condition.
6. The master issues any read/write operation in the known manner.

The master may continue to issue High-Speed read/write operations until a STOP is issued. Issuing a STOP ensures that the bus input filters are set for 1MHz or slower operation. Repeat steps 1 to 6 in the above algorithm to re-enter HS mode after a STOP has been issued.

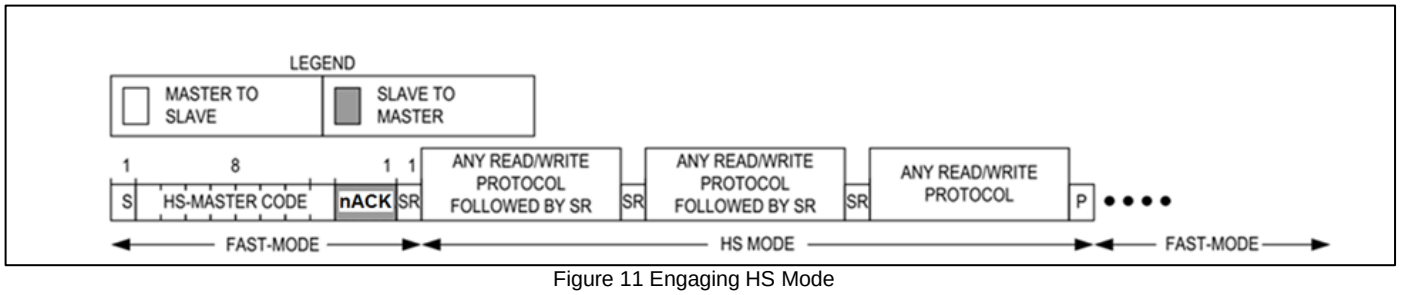


Figure 11 Engaging HS Mode

Registers

Register reset conditions – Registers are reset when VIN = low or EN=low.

Register map - I^2C Slave Address (W/R): 0x86/0x87 (default)

ADDRESS	REGISTER NAME	RESET TYPE	R/W	BIT 7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	RESET VALUE
0x00	DEVICE_ID	TYPE_O	R	RESERVED	VERSION [3:0]				CHIP_REV [2:0]			-
0x01	STATUS	TYPE_O	R	RESERVED	RESERVED	RESERVED	RESERVED	TSHDN	BB_PGn	BB_OVP	BB_OCP	-
0x02	CONFIG1	TYPE_O	R/W	RESERVED	BB_UMODE	BB_RU_SR	BB_RD_SR	BB_OVP [1:0]		BB_AD	BB_FPWM	0x0E / 0x0F
0x03	CONFIG2	TYPE_O	R/W	RESERVED	BB_EN	EN_PD	PG_POL	OCP	RESERVED	RESERVED	RESERVED	0x70 / 0x78
0x04	VOUT	TYPE_O	R/W	RESERVED	VOUT[6:0]							0x28

Device ID Register

ADDRESS	MODE		TYPE: O	RESET VALUE: N/A
0x00	R			
BIT	NAME	POR	DESCRIPTION	
7	RESERVE	0		
6:3	VERSION [3:0]	-	Version 0000b: Plain 0001b: -1Z 0010b: -2Z	
2:0	CHIP_REV [2:0]	-	Chip Revision History 000b: Pass1 001b: Pass2 010b: Pass3 011b: Pass4 100b: Pass5 101b: Pass6 110b: Pass7 111b: Pass8	

Status Register

ADDRESS	MODE		TYPE: O	RESET VALUE: N/A
0x01	R			
BIT	NAME	POR	DESCRIPTION	
7:4	RESERVE	-		
3	TSHDN	-	0: Junction Temperature ≤ 150°C 1: Junction Temperature ≥ 150°C	
2	BB_PGn	-	Buck-boost $\overline{PG}$ Status	
1	BB_OVP	-	Buck-boost OVP Status	
0	BB_OCP	-	Buck-boost OCP Status	

The status register BIT are reset automatically upon fault removal.

Configuration Register 1

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x0E (MODE=0) or 0x0F (MODE=1)
0x02	R/W			
BIT	NAME	POR	DESCRIPTION	
7	RESERVE	0		
6	BB_UMODE	0	Ultrasonic Mode Enable 0: No Ultrasonic Mode 1: Ultrasonic Mode (Fs > 20kHz)	
5	BB_RU_SR	0	Rising Ramp-rate Control 0: 20mV/µs 1: 40mV/µs	
4	BB_RD_SR	0	Ramp-down Slew Rate Control 0: 5mV/µs 1: 10mV/µs	
3:2	BB_OVP_TH [1:0]	11	Output OVP Threshold 00b: No OVP 01b: 110% of VOUT 10b: 115% of VOUT 11b: 120% of VOUT	
1	BB_AD	1	Output Active Discharge 0: Disable Acive Discharge 1: Enable Active Discharge	
0	BB_FPWM	0 or 1	PWM Enable 0: PFM 1: PWM	

Configuration Register 2

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x70 (OCP=0) or 0x78 (OCP=1)
0x03	R/W			
BIT	NAME	POR	DESCRIPTION	
7	RESERVE	0		
6	BB_EN	1	0: Disable Buck-boost Output 1: Enable Buck-boost Output	
5	EN_PD	1	EN Input Pull-down Resistor Enable Setting 0: Disable 1: Enable	
4	PG_POL	1	0: Active Low 1: Active High	
3	OCP	0 or 1	Set the Peak Overcurrent Threshold 0: 2.0A 1: 4.3A	
2:0	RESERVE	000		

Output Voltage Setting Register

ADDRESS	MODE		TYPE: O	RESET VALUE: 0x28		
0x04	R/W					
BIT	NAME	POR	DESCRIPTION			
7	RESERVE	0				
6:0	VOUT [6:0]	010 1000	0x00 = 2.60V	0x20 = 3.24V	0x40 = 3.88V	0x60 = 4.52V
			0x01 = 2.62V	0x21 = 3.26V	0x41 = 3.90V	0x61 = 4.54V
			0x02 = 2.64V	0x22 = 3.28V	0x42 = 3.92V	0x62 = 4.56V
			0x03 = 2.66V	0x23 = 3.30V	0x43 = 3.94V	0x63 = 4.58V
			0x04 = 2.68V	0x24 = 3.32V	0x44 = 3.96V	0x64 = 4.60V
			0x05 = 2.70V	0x25 = 3.34V	0x45 = 3.98V	0x65 = 4.62V
			0x06 = 2.72V	0x26 = 3.36V	0x46 = 4.00V	0x66 = 4.64V
			0x07 = 2.74V	0x27 = 3.38V	0x47 = 4.02V	0x67 = 4.66V
			0x08 = 2.76V	0x28 = 3.40V	0x48 = 4.04V	0x68 = 4.68V
			0x09 = 2.78V	0x29 = 3.42V	0x49 = 4.06V	0x69 = 4.70V
			0x0A = 2.80V	0x2A = 3.44V	0x4A = 4.08V	0x6A = 4.72V
			0x0B = 2.82V	0x2B = 3.46V	0x4B = 4.10V	0x6B = 4.74V
			0x0C = 2.84V	0x2C = 3.48V	0x4C = 4.12V	0x6C = 4.76V
			0x0D = 2.86V	0x2D = 3.50V	0x4D = 4.14V	0x6D = 4.78V
			0x0E = 2.88V	0x2E = 3.52V	0x4E = 4.16V	0x6E = 4.80V
			0x0F = 2.90V	0x2F = 3.54V	0x4F = 4.18V	0x6F = 4.82V
			0x10 = 2.92V	0x30 = 3.56V	0x50 = 4.20V	0x70 = 4.84V
			0x11 = 2.94V	0x31 = 3.58V	0x51 = 4.22V	0x71 = 4.86V
			0x12 = 2.96V	0x32 = 3.60V	0x52 = 4.24V	0x72 = 4.88V
			0x13 = 2.98V	0x33 = 3.62V	0x53 = 4.26V	0x73 = 4.90V
			0x14 = 3.00V	0x34 = 3.64V	0x54 = 4.28V	0x74 = 4.92V
			0x15 = 3.02V	0x35 = 3.66V	0x55 = 4.30V	0x75 = 4.94V
			0x16 = 3.04V	0x36 = 3.68V	0x56 = 4.32V	0x76 = 4.96V
			0x17 = 3.06V	0x37 = 3.70V	0x57 = 4.34V	0x77 = 4.98V
			0x18 = 3.08V	0x38 = 3.72V	0x58 = 4.36V	0x78 = 5.00V
			0x19 = 3.10V	0x39 = 3.74V	0x59 = 4.38V	0x79 = 5.02V
			0x1A = 3.12V	0x3A = 3.76V	0x5A = 4.40V	0x7A = 5.04V
			0x1B = 3.14V	0x3B = 3.78V	0x5B = 4.42V	0x7B = 5.06V
			0x1C = 3.16V	0x3C = 3.80V	0x5C = 4.44V	0x7C = 5.08V
			0x1D = 3.18V	0x3D = 3.82V	0x5D = 4.46V	0x7D = 5.10V
			0x1E = 3.20V	0x3E = 3.84V	0x5E = 4.48V	0x7E = 5.12V
			0x1F = 3.22V	0x3F = 3.86V	0x5F = 4.50V	0x7F = 5.14V

PCB Layout

The AP72200 works at 2A load current, heat dissipation is a major concern in layout the PCB. A 2oz Copper in both top and bottom layer is recommended. Correct PCB layout is critical for proper operation of the AP72200. The following are some general guidelines for the recommended layout:

1. The input and output capacitors should be positioned directly across PVIN-PGND and VOUT-PGND as close to the IC as possible to ensure noise free operation.
2. The ground connections of the input and output capacitors should be kept as short as possible. The objective is to minimize the current loop between the ground pads of the input and output capacitors and the PGND pins of the IC. Use via, if required, to take advantage of a PCB ground layer underneath the regulator.
3. The analog ground pin (GND) should be connected to a large/low-noise ground plane on the top or an intermediate layer of the PCB, away from the switching current path of PGND. This ensures a low noise signal ground reference.
4. Fill the 2ND layer with PGND. Single point connects the GND to 2ND layer PGND.
5. Minimize the trace lengths on the feedback loop to avoid switching noise pick-up. Via should be avoided on the feedback loop to minimize the effect of board parasitic, particularly during load transients.
6. The SW1 and SW2 traces should be short.
7. See figure 11 below for more detail of the recommended layout.

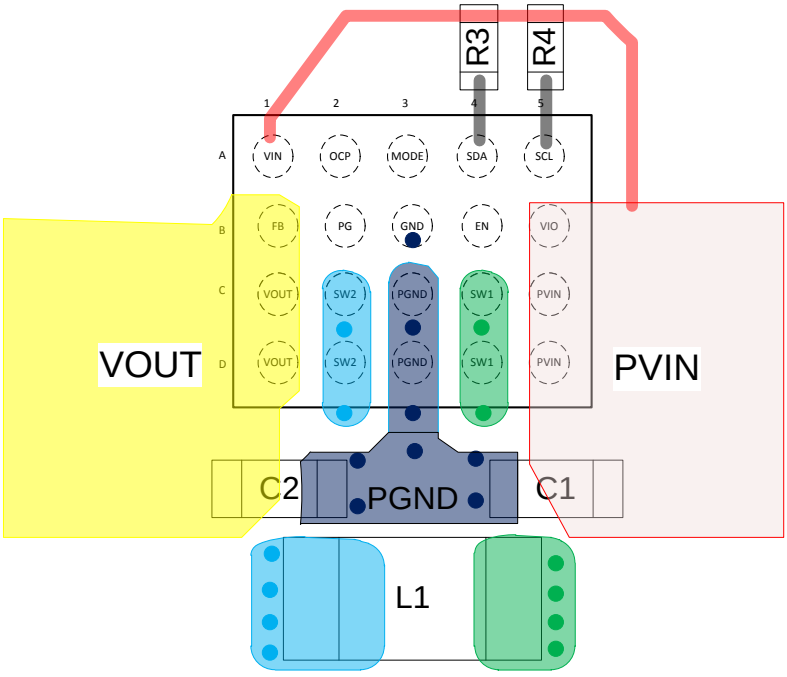
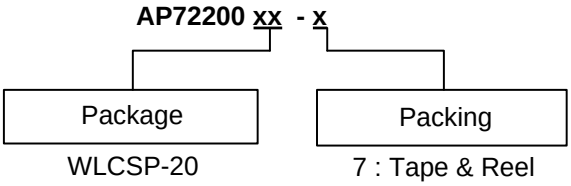


Figure 12 Recommended Layout Design

Ordering Information (Note 9)



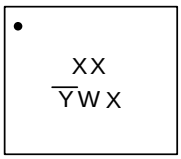
Part Number	Package Code	Package	Identification Code	Tape and Reel	
				Quantity	Part Number Suffix
AP72200CT20-7	W-WLB2118-20	WLCSP-20	D7	3000	-7

Note: 9. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/

Marking Information

(1) W-WLB2118-20

(Top View)



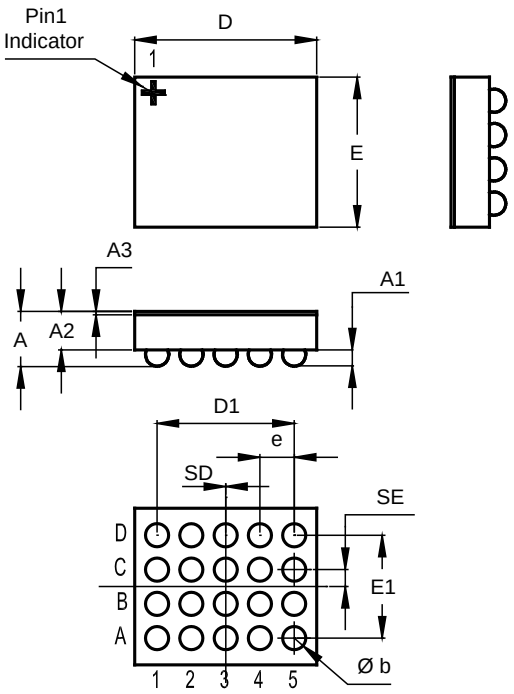
XX : Identification Code
Y : Year 0~9; E~M
W : Week : A~Z : 1~26 week;
a~z : 27~52 week; z represents
52 and 53 week
X : Internal Code

Part Number	Package	Identification Code
AP72200CT20-7	W-WLB2118-20	D7

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-WLB2118-20

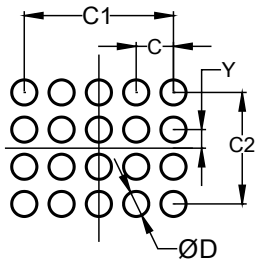


W-WLB2118-20			
Dim	**Min**	**Max**	**Typ**
A	0.59	0.69	0.64
A1	0.17	0.21	0.19
A2	0.45 REF		
A3	0.012	0.032	0.022
b	0.24	0.30	0.27
D	2.10	2.15	2.125
D1	1.550	1.650	1.600
E	1.725	1.775	1.750
E1	1.150	1.250	1.200
e	0.40 BSC		
SD	0.00 BSC		
SE	0.20 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

W-WLB2118-20



Dimensions	Value (in mm)
C	0.400
C1	1.600
C2	1.200
D	0.270
Y	0.200

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